Abstract - This paper presents the study and simulation of a new family of symmetrical hybrid multilevel inverters based on Cuk and Zeta converters, able to high step up/down voltages, primarily focused on applications for non-conventional renewable energy systems where DC voltage link is of low value. The main characteristics of these circuits, it is possible to obtain output voltages higher and lower than the input. Finally, due to the pattern of drive used, it is possible to obtain a low distortion in the output voltage.

**Keywords:** DC-AC converters, Quadratic converters, multilevel inverters.

I. INTRODUCTION

The use of non-conventional renewable energy is something of vital importance today. It is known that electricity generation through plants that burning fossil fuels is one of the deterioration causes of planet earth, causing effects such as global warming, among others. Conventional energy resources such as fossil fuels are running out very quickly, and that is why, energies such as photovoltaic, wind or that obtained through a fuel cell are the options being considered for solve an energy shortage in the future [1].

Among the different technologies using existing renewables, the one that has matured and evolved, increasing its reliability, efficiency and profitability, is definitely the wind and solar energy [2] [3]. In particular photovoltaic (PV) has application in autonomous systems generally away from the distribution lines due to its geographical location, for which represent the most economical option. While direct costs not yet compete with conventional generation technologies, some recent economic evaluations show that, if one takes into account the indirect costs of the generation and distribution of electric power, photovoltaic systems (PVS) are near economic viability in systems that interact with the electrical network, i.e. the network interconnected systems. [4]

Figure 1 shows the block diagram of a photovoltaic system interconnected to the network. Basically, a photovoltaic system interconnected to the network, is a system that operates in parallel to it, that is, two systems feeding a load. These systems are also called interactive systems, since the user (or load) can be powered both the network, such as the photovoltaic system or both.

The idea it is interconnected in a parallel manner to the network, is that, given a potential scenario in which the photovoltaic system generates more energy than required by the load, then, can be injected to the same network, thus the users not only get the free and clean energy; also is selling its surplus power.

The problem that exists in photovoltaic systems is that each panel generates a DC voltage of very low value as to make direct use of this to interface to the network or for home use [5]. That is why it takes a stage that conditions the way of energy delivered by the PV array to give a fair use the basic requirements demand. That is, it requires an intermediate step between the PV system and the user, which ensures voltage waveform quality and increased in magnitude compared to the voltage delivered by the photovoltaic system. This stage is called "power conditioning stage," and is the one responsible for storing, invert, raise and filter the voltage delivered by the PV system.

The multi-stage and single-stage inverters are the most used topologies to obtain an accord voltage to domiciliary requirements. The difference is just that multi-stage inverters, require several intermediate blocks to do the work of raising and invert the input voltage, which reduces the efficiency of the system.

Instead single-stage topologies perform work to raise and invert the input voltage in only one stage. This topology is based on DC-DC boost converters. Inside mono-stage boost inverters topologies, there is the proposed circuit by [7], and is shown in Figure 2. Inside the multi-stage inverters, the topologies DC-DC-AC, AC-AC DC and DC-AC-DC-AC, are the most used [5].
Figure 3 shows the multi-stage topologies used to invert and raise the input voltage supply systems with systems based on non-conventional renewable energies.

This paper proposes a new family of symmetric hybrid multilevel inverter circuits with the advantage of being Step-Down/Step-Up structures with quadratic gain, i.e., with a gain of AC output voltage much greater than one. Therefore it is very convenient generation applications unconventional alternatives such as photovoltaic (PV) power generation systems or based on fuel cells for smart distribution networks applications.

![Figure 3 Multi-stage inverters: (a) DC-DC-AC topology  (b) DC-AC-AC topology  (c) DC-AC-DC-AC topology.](image)

The great advantage of the proposed topologies is that it are just of one stage, so it can be classified like single-stage inverters. Also, the voltage gain is quadratic, allowing obtaining an output voltage several times greater than the input voltage. The modulation to use is not complex and allows various types of control.

II. DERIVATION OF QUADRATIC-GAIN SYMMETRICAL HYBRID MULTILEVEL DC-AC CONVERTERS

The proposed inverters are based directly of Zeta and Cuk circuits with three voltage levels and quadratic gain. These are shown in Figure 4 [11].

![Figure 4. DC-DC quadratic Converters: (a) Quadratic Cuk converter (b) Quadratic Zeta converter.](image)

The waveform of the $V_{AB}$ voltage of quadratic Cuk converter of three levels to when the switches are being driven by single pulse, it is shown in Figure 5.

![Figure 5 Waveform of the $V_{AB}$ voltage.](image)

In the same way, for the quadratic Zeta converter of three levels, the voltage $V_{AB}$, obtaining to when switches are being driven by single pulse, it is of the same shape as in the case of the Cuk converter of three levels, but with
positive polarity. To operate as on inverters, the converters presented above must meet three basic operating requirements, these are:

a) Bidirectional current switches in the cell;
b) Bidirectional output voltage;
c) Voltage and current average zero in the load, which means that the output capacitors must be loaded symmetrically.

Because of these restrictions is that you must make changes to the structures previously presented in order to make them comply with the characteristics of a typical inverter topology.
First, to meet the conditions of bidirectional current, it is necessary operate the circuit with switches that meet this condition. This is shown in Figure 6 (a) and (b), where shows the Cuk and Zeta quadratic circuits with those amendments, where the load has been generalized like a bidirectional current source and is not shown the output filter of each converter. Bidirectionality of the load voltage is achieved by a bridge inverter connected between the inverter output and the load. Depending on the type of inverter, is possible achieve two different configurations: half bridge configuration (Figure 7 (a) and 7 (b)), and full bridge configuration (Figure 8 (a) and 8 (b)).
The output voltage of inverters to when their switches are being driven by single pulse is shown in Figure 9.

The switches $S_4$ to $S_1$ operate in high frequency (in the text are referred to as fast switches) technology and may be IGBT, MOSFET or Bipolar. The switches $S_5$ to $S_8$ operate at low frequencies (so it will be called slow switches), and operating for half cycle load voltage.

The technology to implement in these switches may be of GTO or IGCT. Fast switches Cuk converter, must withstand a high reverse voltage that’s equals $v_{c2}$, while in the Zeta converter is $v_{c2} + E/2$. H-bridge switches in the Cuk converter, must withstand a high reverse voltage equals $2v_c$, while in the Zeta converter switches, withstand a maximum voltage equal to $2v_c + E$. Due to the fact which the output voltage varies quadratically with respect to the input voltage, so does the current input, which make increase the conduction losses.

$$v_{c2} = \frac{E}{2}$$

$$2v_c$$

$$2v_c + E$$

Due to the fact which the output voltage varies quadratically with respect to the input voltage, so does the current input, which make increase the conduction losses.

III. MODULATION STRATEGY.

The modulation strategy of the converters studied is based on the PWM technique known as PSD (Phase Shift Disposition). In this, the command signals of each fast switch ($S_1$ a $S_8$) are obtained from the comparison between a sinusoidal modulating signal $v_m$, and two triangular carrier signals $v_{11}$ and $v_{12}$. $180^\circ$ out of phase from one another. The command signals of H Bridge, are obtained from the comparison between the modulating signal $v_m$, and the zero voltage level. $v_m$ and $v_{11}$ signals and output pulses of each circuit of the modulation scheme are shown in Figure 10 (a), (b) and (c) respectively. The frequency index is chosen $m_T = 5$. An odd value is justified, because for these values of frequency rates it is obtained an energy balance in the theoretically perfect converter elements.

IV. ANALYSIS OF THEORETICAL OUTPUT VOLTAGE OF PROPOSALS TOPOLOGIES.

This section shows the study of the theoretical output voltages, the harmonic spectrum and THD analysis of the circuits shown in previous sections. The procedure for calculating the expressions shown below is shown in [5]. Furthermore, it displays the average value expression of voltage on the capacitors of the inverter. All expressions are derived without considering the voltage ripple on the capacitors of the inverter.

A. Output voltage of the H-Bridge topologies

The expression that defines the output voltage of the H-bridge topologies proposed (Cuk and Zeta) is given by:

$$v_{out} = \frac{E}{2}$$

$$2v_c$$

$$2v_c + E$$

Fig. 10. Modulation Strategy (a) modulating and carrier signals (b) command pulses (c) modulation logic circuit.
\[ V_{out} = \frac{E_m}{(1-m_{\text{mod}})} \sin(\omega t) + \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \frac{2E}{(1-m_{\text{mod}})^2} J_n(n \pi m) \left[ \sin(\omega_{im} t + \omega t) \right] \]

(1)

Where \( m_{\text{mod}} = 2m_i / \pi \), \( \omega_s = 2\pi f_s \), \( \omega_0 = 2\pi f_0 \), and \( J_n(n \pi m_i) \) represents the Bessel function of order \( v \) and argument \( n \pi m_i \).

Observing the expression (1), it may be noted that the harmonic components are in sidebands around even multiples of the switching frequency, a fact that will be noted below in the section V [Fig.18 (b)]. Figure 10 shows the graph of equation (1) normalized to source voltage \( E/2 \), and to a modulation index \( m_i = 0.97 \). The amplitudes of the fundamental and harmonic components are shown in Table I and shown in Figure 11. Figure 12 shows the THD variation of the output voltage as a function of modulation index \( m_i \). For the chosen index, percentage THD is a 28.36%.

<table>
<thead>
<tr>
<th>Component</th>
<th>Amplitude</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental ( A_1 )</td>
<td>( \frac{E m_i}{(1-m_{\text{mod}})^2} )</td>
<td>( \omega_1 )</td>
</tr>
</tbody>
</table>

Harmonic \( A_{0,v} \)

\( n = 0, 2, 4, ... \)
\( v = 1, 3, 5, ... \)

\[ \frac{2E}{(1-m_{\text{mod}})^2} [J_v(n \pi m_i)] \] \( \pm \omega_1 \pm n \omega_2 \)

B. Output voltage Half-bridge topologies

The expression that defines the output voltage of the Cuk and Zeta Half-bridge topologies is given for:

\[ V_{out} = \frac{E m}{(2\pi-m_{\text{mod}})^2} \sin(\omega t) + \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \frac{E}{(1-m_{\text{mod}})^2} J_n(n \pi m) \left[ \sin(\omega_{im} t + \omega t) \right] \]

(2)

From (2) it is possible to note that the harmonic components are in sidebands around multiples of the switching frequency, a fact that will be noted later in Section V [Fig.19 (b)]. Figure 13 shows the graph of the expression (2) normalized to source voltage \( E/2 \), for a modulation index equal to 0.97. The amplitudes of the fundamental and harmonic components are set forth in Table II and shown in Figure 14. Figure 15 shows the variation of voltage’s THD as a function of index modulation \( m_i \). For the chosen index, the percentage of THD is a 55.034%.
The average voltage over $C_{a1}$ and $C_{a1'}$, is given by the expression (4):

$$V_{ca1} = \frac{\left(\frac{E}{2}\right) m_1}{1 - \frac{2m_1}{\pi}}$$  \hspace{1cm} (4)$$

This expression is valid for both inverters Cuk; to five and three levels.

**D. Average voltage on the capacitors (Zeta topologies)**

The average voltage on the capacitors $C_{a2}$ and $C_{a2'}$, is given by the following expression [5]:

$$V_{Ca1} = \frac{\left(\frac{E}{2}\right) \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (5)$$

The average value of the voltage over $C_{a1}$ and $C_{a1'}$, given by the expression (6):

$$V_{Ca2} = \frac{\left(\frac{E}{2}\right) \frac{2m_1}{\pi} \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (6)$$

This expression is valid for both inverters Zeta; to five and three levels.

**E. Maximum reverse voltage of the switches (Cuk topologies).**

For switches $S_1 - S_4$, the maximum reverse voltage that must support is given by the following expression:

$$V_{S_1-S_4,max} = V_{Ca2} = \frac{\left(\frac{E}{2}\right) \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (7)$$

For H-bridge switches, the maximum reverse voltage that must support is:

$$V_{S_{H-bridge,max}} = 2 \cdot V_{Ca2} = \frac{2 \left(\frac{E}{2}\right) \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (8)$$

**F. Maximum reverse voltage of the switches (Zeta topologies).**

For switches $S_1 - S_4$, the maximum reverse voltage that must support is given by the following expression:

$$V_{S_1-S_4,max} = V_{Ca2} + \frac{E}{2} = \frac{\left(\frac{E}{2}\right) \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (9)$$

For H-bridge switches, the maximum reverse voltage that must support is:

$$V_{S_{H-bridge,max}} = 2 \cdot V_{Ca2} + E = \frac{2 \left(\frac{E}{2}\right) \frac{2m_1}{\pi}}{\left(1 - \frac{2m_1}{\pi}\right)}$$  \hspace{1cm} (10)$$

In it can be observed that the voltages over devices are depending of $m_1$.
V. SIMULATION

In this section are shown the results of numerical simulations carried out in PSIM environment, family of converters in full and half bridge. The design specifications of each family of circuits are shown in Table III. All circuits are considered ideal. In Figure 16 (a) is shown the output voltage waveform of the Cuk H-bridge inverter, which is analogous to the H-bridge Zeta. The waveform has five voltage levels. Figure 17 (b) shows the harmonic spectrum of the output voltage, where the harmonics are more influential to twice the switching frequency. From Fourier analysis, it appears that the maximum fundamental output voltage is 312 (V), taking a gain of 2.4xE for $m_f = 0.71$.

In Figure 18 (a) is shown the voltage waveform output Cuk Half-bridge inverter, which is analogous to the Half-bridge Zeta. The Waveform has three voltage levels. Figure 18 (b) shows the harmonic spectrum where most influential harmonics are multiples of the switching frequency.

### Table III

| Design specifications for full-bridge converters (FB) and half-bridge (HB) |
|---|---|---|---|
| DC link Voltage $E$ | Value $FB$ | Value $HB$ |
| Output power $P_o$ | 10(kW) | 10(kW) |
| Output frequency (fundamental) $f_o$ | 50(Hz) | 50(Hz) |
| Fundamental load voltage (RMS) $V_{f1 RMS}$ | 220(V) | 220(V) |
| Displacement factor (load) $\cos( \phi)$ | 0.8 | 0.8 |
| Modulation index $m_l$ | 0.71 | 0.9 |
| Capacitors Inverter (first stage) $C_{c_{a1}}$ | 4.93(mF) | 6.24(mF) |
| Inverter input inductor $L_{1} - L_{1}'$ | 7.54(mH) | 12.1(mH) |
| Inductor of the second stage inverter $L_{a} - L_{a}'$ | 10.3(mH) | 21(mH) |
| Output capacitor $C_{a1} - C_{a1}'$ | 4.2 (mF) | 5.53 (mF) |
| Switching frequency $f_s$ | 1.65(kHz) | 1.65(kHz) |
| Load resistance $R_o$ | 3.1(Ω) | 3.1(Ω) |
| Load inductance $L_o$ | 7.4(mH) | 7.4(mH) |

We can see that in the output voltages of three and five levels appears a low frequency ripple, which is due for two main reasons: one is by the modulation itself, and the other is because the capacitors have a finite value (for a more detailed analysis, see reference [5]). This ripple is reflected in the output voltage as a third harmonic component.

From Fourier analysis, it appears that the maximum fundamental output voltage is 315.86 (V), taking a gain input value of 2.437xE for $m_l = 0.8924$.

H-bridge topologies, presents an output voltage THD of 28.99%. For half-bridge topologies, you get a THD in the output voltage of 55.21%.

VI. CONCLUSIONS

In this paper a family of symmetrical hybrid multilevel inverters was introduced, able to obtaining quadratic gain. The main feature of these circuits is that they operate with hybrid modulation (derived from the
PSD-PWM modulation), occupying both rapid and slow circuit.

Two types of topologies Cuk and Zeta versions: One in half-bridge configuration and the other in full-bridge configuration are presented. The simulations show that the half-bridge topologies have three voltage levels and harmonics around the switching frequency. For full-bridge topologies, showed five voltage levels and harmonics around even multiples of the switching frequency. The voltage gain has a quadratic dependence with the modulation index $m_i$.

They were also presented Fourier expressions that represent the output voltages of the proposed topologies, which are in good agreement with numerical simulations obtained. From THD analysis, it is can be observed that this decreases as the modulation index increases.

In relation to voltage stresses, for both topologies full-bridge and half-bridge, the fast switches must endure reverse voltage greater than half the DC link (E/2), varying quadratically with respect to the chosen modulation index. For H-bridge switches, these must withstand voltages greater than the DC-link (E), also quadratic variation with the modulation index.

REFERENCES


